

1st Call for Papers

2008 International Workshop on DIELECTRIC THIN FILMS FOR FUTURE ULSI DEVICES — SCIENCE AND TECHNOLOGY —

(November 5-7, 2008, Tokyo Institute of Technology, Tokyo, Japan)

Sponsored by
The Japan Society of Applied Physics

Cosponsored by
Association of Super-Advanced Electronics Technologies (ASET), Japan

Technically Cosponsored by
IEEE Electron Devices Society

SCOPE:

The 2008 International Workshop on “Dielectric Thin Films for Future ULSI Devices: Science and Technology” (IWDTF-08) will be held at Tokyo Institute of Technology, Meguro-ku, Tokyo, Japan, on November 5-7, 2008. The IWDTF started in 1999, based on a domestic annual workshop on ultrathin silicon dioxide films. In succession to the second (IWDTF-04, Tokyo) and the third (IWDTF-06, Kawasaki) workshops, the IWDTF-08 will focus on the science and technologies of gate dielectric films for MOS devices, such as ultrathin SiO₂, SiON, high-k gate dielectrics, and ferroelectric films. The topics on other technologies involved in the advanced gate stacks, which include metal gate electrodes and high-mobility channel materials, will also be discussed. The IWDTF will provide a great opportunity for information exchange and discussions at forefront of the researches on future ULSI. The papers on both experimental and theoretical studies, for the deep understanding of the properties of gate dielectric films and their interfaces, are welcomed. The workshop will consist of invited and contributed talks, and poster presentations. Selected topics of current interests will be reviewed by several invited talks.

Papers are solicited in, but not limited to, the following area:

- Ultrathin silicon dioxide, oxynitride and oxide-nitride composite dielectrics
- High-k gate dielectrics
- Metal gate electrodes
- Mobility enhancement technology
- Ferroelectric and high-k films for memory applications
- Growth and related process of gate dielectric films
- Electrical characterization of gate dielectrics
- Gate dielectric wearout and reliability
- Characterization and control of gate dielectric/Si interface
- Surface preparation and cleaning issues for gate dielectrics
- Dielectric reliability related to process integration
- Theoretical approaches to gate dielectrics/Si structure

Invited keynote speakers (tentative):

H. Watanabe (Selete) and S. Biesemans (IMEC)

Workshop Language:

The official language of the workshop is English.

Submission of Papers:

Paper acceptance is based on the submitted abstracts. The work must be original and unpublished. The prospective authors are requested to submit abstract(s) (in a WORD or PDF file), two pages in length, including all figures and tables, by **July 25, 2008** to the workshop website at <http://home.hiroshima-u.ac.jp/iwdtf/>.

The two-page abstracts must be written in English and typed in an area of 8.5 × 11 inches or A4 size. The first page must be headed by the title of the paper, author(s), affiliation(s), address, telephone number, fax number, e-mail address of the corresponding author. The abstract must clearly and concisely state the specific results of the work and its originality. The detailed information about the format will be provided at the workshop website. Papers to be presented at the workshop will be selected by the program committee on the basis of the content of submitted abstracts. The decision will be notified by e-mail until the beginning of September 2008. All contributors will be requested to give either an oral presentation conforming to 20 minutes format or poster presentation. Please note that no submission by Fax will be accepted.

Submission of Full-Papers to the Special Issue of JJAP:

Authors of papers accepted in IWDTF-08 are encouraged to submit the original and significant part of the papers to the Special Issue of the Japanese Journal of Applied Physics (JJAP), which will be published in May 2009. The deadline of the paper submission is October 31, 2008. Please refer to the IWDTF-08 website for the detailed information. Those who wish to submit a paper to the special issue should follow the instructions for preparation of manuscript for JJAP. Please note that the manuscript will be published after the usual review process in JJAP. The special issue is not just proceedings of IWDTF-08.

Registration:

Registration for the IWDTF-08 should be made on the workshop website.

Participants	Pre-registration (On or before October 10, 2008)	On-site Registration (After October 10, 2008)	Banquet
Regular	¥30,000	¥35,000	¥5,000
JSAP or IEEE member	¥25,000	¥30,000	¥5,000
Student	¥10,000	¥10,000	¥5,000

Payment should be made in Japanese yen by bank transfer to the following;

A/C Name: 2008IWDTF SHUN-ICHIRO OHMI, A/C No.: 1683758

Bank Name : MIZUHO BANK, LTD. (SWIFT BIC : MHBKJPJT)

Branch Name : Nagatsuta Branch

4-1-23 Nagatsuta, Midori-ku, Yokohama, 226-0027, Japan

For on-site registration, credit card of Master, VISA and AMEX are also acceptable.

*No cancellation will be accepted after October 15, 2008.

The registration fee includes admission to the workshop sessions, a copy of abstract book and a CD-ROM.

The banquet will be held in the evening on November 5, 2008.

Organizing Committee

Chairperson: S. Zaima (Nagoya Univ.)

Members: K. Yamabe (Univ. of Tsukuba), T. Masuhara (ASET), Y. Nishioka (Nihon Univ.), K. Maeguchi (SIRIJ),
K. Yamada (Waseda Univ.), A. Toriumi (Univ. of Tokyo)

Steering Committee

Chairperson: Y. Nara (Selete)

Vice Chairperson: S. Ohmi (Tokyo Tech)

Members: K. Kita (Univ. of Tokyo), S. Miyazaki (Hiroshima Univ.), N. Miyata (AIST), A. Sakai (Osaka Univ.),
H. Watanabe (Osaka Univ.), T. Watanabe (Waseda Univ.), C. Kaneta (Fujitsu Labs.)

Program Committee

Chairperson: J. Yugami (Renesas)

Vice Chairperson: Y. Takakuwa (Tohoku Univ.)

Members: Y. Akasaka (Tokyo Electron), T. Chikyo (NIMS), K. Eriguchi (Kyoto Univ.), T. Hamada (Univ. of Tokyo),
K. Hirose (ISAS), S. Horii (Hitachi Kokusai Electric), S. Inumiya (Toshiba), S. Hayashi (Matsushita Electric),
H. Kageshima (NTT), K. Kakushima (Tokyo Tech), Y. Kamakura (Osaka Univ.), K. Kobayashi (Tokai Univ.),
T. Matsuki (Selete), S. Migita (AIST), K. Muraoka (Toshiba), T. Nabatame (ASET), Y. Nishida (Renesas),
A. Nishiyama (Toshiba), M. Niwa (Matsushita Electric), H. Nohira (Musashi Inst. Technol.), K. Torii (Hitachi),
S. Samukawa (Tohoku Univ.), K. Sasakawa (KOBELCO), Y. Shimamoto (Hitachi), K. Tsutsui (Tokyo Tech),
K. Shiraishi (Univ. of Tsukuba), A. Tachibana (Kyoto Univ.), M. Takayanagi (Toshiba), T. Tatsumi (NEC),
E. Tokumitsu (Tokyo Tech), Y. Tsuchiya (Tokyo Tech), S. Tsujikawa (Sony), T. Yamamoto (Toray)

Important Dates

Abstract Deadline:	July 25, 2008
Notification of Acceptance:	September 5, 2008
Pre-Registration Deadline:	October 7, 2008
Workshop:	November 5-7, 2008