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32-Gbit/s CMOS Receivers in 300-GHz Band

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SUMMARY This paper presents low-noise amplifier (LNA)-less 300-GHz CMOS receivers that operate above the NMOS unity-power-gain frequency, f_{max}. The receivers consist of a down-conversion mixer with a doubler- or tripler-last multiplier chain that upconverts an $LO^{1/n}$ signal into 300 GHz. The conversion gain of the receiver with the doubler-last multiplier is −19.5 dB and its noise figure, 3-dB bandwidth, and power consumption are 27 dB, 27 GHz, and 0.65 W, respectively. The conversion gain of the receiver with the tripler-last multiplier is −18 dB and its noise figure, 3-dB bandwidth, and power consumption are 25.5 dB, 33 GHz, and 0.41 W, respectively. The receivers achieve a wireless data rate of 32 Gb/s with 16QAM. This shows the potential of the moderate-f_{max} CMOS technology for ultrahigh-speed THz wireless communications.

key words: *Receiver, CMOS integrated circuits, terahertz, frequency conversion mixers, frequency multipliers, amplifiers, quadrature amplitude modulation*

1. Introduction

The unallocated and underutilized terahertz (THz) frequencies above 275 GHz are expected to enable ultrahigh-speed broadband wireless communications [1]–[3]. The potential challenges include not only the design of THz transmitters (TXs) and receivers (RXs) but also the development of the baseband circuitry that can handle extreme data rates. Since compound-semiconductor technologies offer significantly higher unity-power-gain frequency, f_{max}, than CMOS technologies, the former are clearly a better choice in terms of RF performance. However, because of the very intensive signal processing required, CMOS technology is the only choice for the baseband. This, in turn, provides strong motivation for exploring the possibilities of realizing CMOS THz front-ends. If the highest f_{max} of a FET is sufficiently higher than the operating frequency, a power amplifier (PA) and low-noise amplifier (LNA) can be designed. Further, the conventional LNA-first architecture can be adopted in the RX (shown in Fig. 1 (a)). The overall noise figure is effectively lowered by an LNA in this architecture, according to the Friis formula (1).

$$\mathrm{NF_{total}} = \mathrm{NF_1} + \frac{\mathrm{NF_2} - 1}{G_1} + \frac{\mathrm{NF_3} - 1}{G_1 \times \mathrm{G_2}} + \cdots + \frac{\mathrm{NF}_n - 1}{G_1 \times G_2 \times \cdots \times G_n} \quad (1)$$

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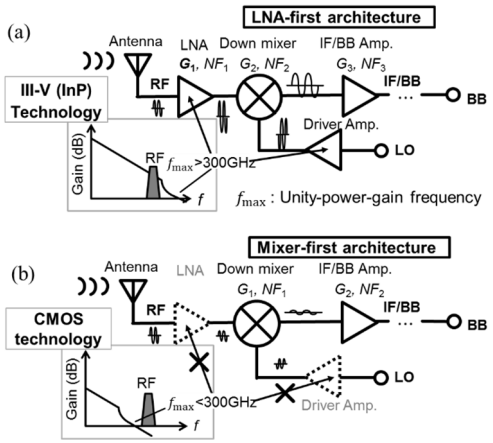


Fig. 1 Receiver architectures. (a) LNA-first architecture for below-f_{max} operation. (b) Mixer-first architecture for near- or above-f_{max} operation.

However, most CMOS technologies offer f_{max} below THz frequencies. Developments in PAs, LNAs, and driver amplifiers (DAs) in the THz band front-ends by the CMOS technology are highly challenging; therefore, LNA-less architectures should be adopted in the RX (shown in Fig. 1 (b)).

Recently, QAM-capable 300-GHz TXs that operate above f_{max} were developed using a 40-nm CMOS process [4]–[6]. The cubic and square mixers, which are gate-pumped subharmonic- and harmonic-mixers, respectively, are located at the last stage of the TX. These mixers generate 300 GHz of carrier frequency with high power and good linearity. Nevertheless, THz RXs have also been developed using compound semiconductors, silicon germanium, and Si CMOS technologies [7]–[12]. To diffuse THz wireless communications, a receiving performance with high data rate is required. In addition, low power consumption is also crucial.

Herein, we present 300-GHz RXs in 40-nm CMOS, operating above f_{max}. The RXs consist of a down-conversion mixer with a doubler- or tripler-last multiplier chain that upconverts the LO signal to approximately 300 GHz [13], [14]. The RXs achieve a wireless data rate of 32 Gb/s with 16QAM. It shows the potential of moderate f_{max}, which is approximately 200–300 GHz in the CMOS technology to be used for ultrahigh-speed THz wireless communications.

2. Design

Figure 2 shows the state-of-the-art of LNA-less RX architecture. Subharmonic-mixer (SHM)-first, and fundamental-mixer-first architectures can be considered as typical RXs operating above f_{max}. An SHM has the advantage of using a lower LO frequency. However, the N-push operation is performed by itself and the conversion gain would be low [15], [16]. If the signal with the same power comes from the driver amplifier at a frequency below f_{max}, the frequency multiplier would generate a larger output power. Therefore, in general, the output power and conversion gain of an SHM are lower than those of a fundamental mixer, and the total noise figure tends to deteriorate according to (1). We adopted the fundamental-mixer-first architecture for our 300-GHz RXs for obtaining possibly higher conversion gains.

2.1 300-GHz Down-Conversion Mixer

Figure 3 (a) shows the schematic diagram of the 300-GHz down-conversion mixer, which is the double-balanced fundamental mixer consisting of four 32-μm-wide transistors. The LO and RF signals are applied to their gates and drains, respectively. The matching networks are implemented using the transmission line (TL) open- and short-circuited stubs used for the capacitive impedance matching (in Fig. 3 (b)). A short stub, TL1, is also used for the gate bias line of the mixer. The simulated results of the load pull analysis sweeping the terminating impedance of the LO and RF are shown in Fig. 3 (b). The input powers of the LO and RF are 0 and −40 dBm, respectively, with the frequency of 295 GHz and 305 GHz, respectively. Further, it indicated that the impedance matching can be realized with these matching circuits and the optimal conversion gain of approximately −12 dB is estimated in this input condition. Figures 3 (c) and (d) show the simulated results of the linearity depending on the LO power, and the frequency response of the conversion gain and LO-RF isolation depending on the RF frequency, respectively. These results indicated that (I) a higher LO power is required to obtain a higher conversion gain and (II) a wide bandwidth could be achieved if the optimal input power was supplied in the frequency band. The power consumption is estimated to be approximately 5.6 mW. The LO-RF isolation is estimated to be approximately 35.6 dB, which indicates that an LO leak of approximately −35 dBm would be emitted when the LO input power is 0 dBm. The 300-GHz RXs are designed by combining the down-conversion mixer with the following LO multipliers.

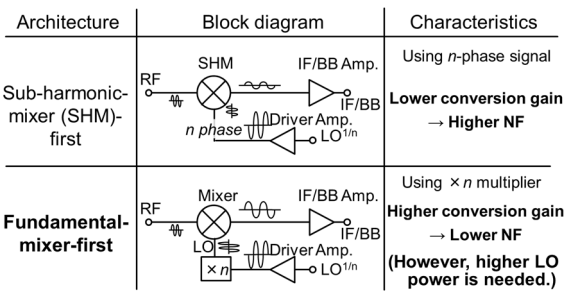


Fig. 2 State-of-the-art LNA-less RX architecture.

2.2 LO Driver

In the fundamental mixer above, a higher LO power is required for achieving a higher conversion gain. To design the 300-GHz LO driver, doubler- and tripler-last architectures that upconvert the based $LO^{1/n}$ signals with frequencies of 150 GHz and 100 GHz are recommended. The architectures are almost similar to the QAM-capable 300-GHz CMOS TXs composed of the square and cubic mixer, which is a type of gate-pumped mixer, at the last stage [4], [6]. The difference is that the multiplier is used at the last LO stage of the RX while the gate-pumped mixer is used at the last stage of the TX. Further, the function and demand of each are different. In the case of the TX, the $LO^{1/n}$ and IF signals are input simultaneously to its gate-pumped mixers, and the combined signal is used as the RF signal (shown in Fig. 4 (a)). Therefore, a high output power and linearity are required. However, in the case of the RX where only the $LO^{1/n}$ signal is input to its multiplier, a high saturation power is exclusively required (shown in Fig. 4 (b)). The difference in the performance of the multipliers and driver amplifiers in each frequency band affects the total performance.

2.2.1 Doubler and Tripler

Figures 5 (a) and (b) show the schematics of a single-ended doubler and differential tripler upconverting the frequencies of 150 GHz and 100 GHz into 300 GHz, respectively. To examine the actual performance in each frequency band, the

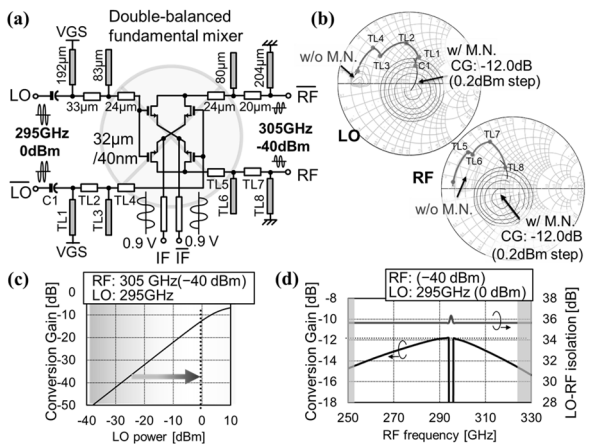


Fig. 3 (a) Schematic diagrams of 300-GHz double-balanced fundamental mixer. Simulated results of (b) impedance matching process at 300 GHz and the load-pull analysis, (c) linearity depending on the LO power, and (d) frequency response of the conversion gain and LO-RF isolation depending on the RF frequency. ((b)–(d) input powers of LO and RF are 0 and −40 dBm at the frequency of 295 GHz and 305 GHz)

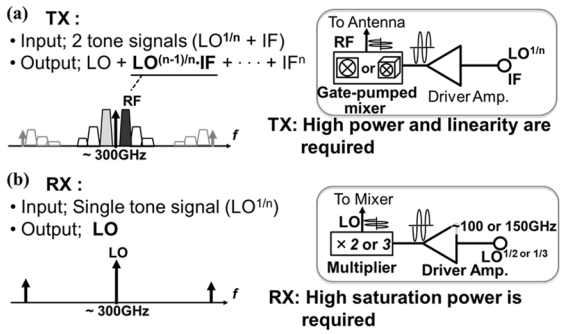


Fig. 4 Schematic configurations of the I/O spectrums and the block diagrams of (a) THz TX with CMOS technologies [4], [6] and (b) LO multiplier of RX.

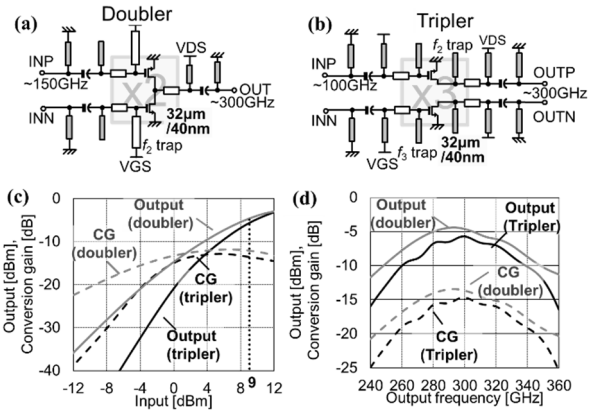


Fig. 5 Schematic diagrams of (a) doubler and (b) tripler. Simulated results of the (c) linearity and (d) frequency response.

parasitic components around the MOSFET, which are estimated by electromagnetic (EM) simulations, are included. The matching circuits are used to design the transmission line (TL) shunt stubs. The TL filters that suppressed the unwanted harmonic signals are designed with the open-circuited stubs of length $\lambda/4$ (λ is the wavelength of each harmonic tone). Figure 5 (c) shows the simulated results of the output powers and conversion gains of the doubler and tripler depending on the input power at the frequency of 150 GHz and 100 GHz, respectively. The output power of the doubler and tripler at an input of 9 dBm, which is considered the saturation power of DAs as mentioned below, are −4.8 dBm and −5.7 dBm, respectively. Figure 5 (d) shows the simulated results of the frequency response of the output power with the input power of 9 dBm. It shows that the bandwidth of the doubler is wider than that of the tripler by approximately 10 GHz. These results indicated that the doubler has an advantage in terms of output power and bandwidth if the same input power could be generated by a DA.

2.2.2 Driver Amplifiers

The output power of the multiplier is strongly dependent on the input $LO^{1/n}$ power influenced by the DA performance. Figure 6 (a) shows the schematics of a single-stage DA. The differential DA with a capacitive cross-coupling technique

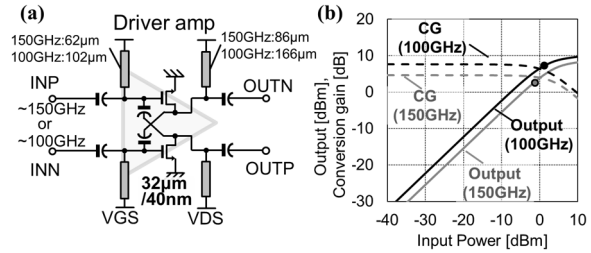


Fig. 6 (a) Schematic diagram of a DA stage, and (b) simulated results of the linearity of the 150-GHz and 100-GHz DAs.

Table 1 Performance summary of a stage of the driver amplifiers.

Freq [GHz]	Gain [dB]	OP1dB [dBm]	IP1dB [dBm]	Psat [dBm]
150	5.0	3.5	-1.0	8.0
100	7.5	5.4	1.8	9.5

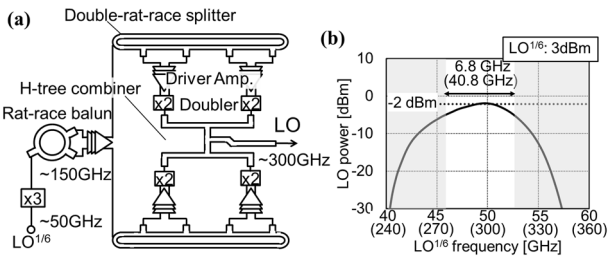


Fig. 7 (a) Schematic diagram of the doubler-last LO multiplier chain and (b) simulated result of frequency response of output power.

consists of the common-source stage with two 32-um-wide transistors. For a fair comparison, the performances of the 150-GHz and 100-GHz DAs are investigated using the same amplifier stage. The matching circuits, which are designed to adopt a compact layout technique for a cascode differential amplifier [17], are adjusted for obtaining the optimal power in each frequency band. The simulated results and performance summary of each amplifier, which include the parasitic components around the FET and TLs, are shown in Fig. 6 (b) and Table 1, respectively. The gains of 5.0 dB and 7.5 dB and the saturation powers of 8.0 dBm and 9.5 dBm are estimated by the 150-GHz and 100-GHz DAs, respectively. It indicated that the performance of the 150-GHz amplifier is worse than that of the 100-GHz amplifier because of the higher operating frequency. To obtain a higher $LO^{1/n}$ power in the 150-GHz DA, we expected that a larger number of the cascode stage is required as well as the power stage composed of the larger FET size, for higher gain and saturation power.

2.2.3 LO Multiplier Chains

Figure 7 (a) shows the schematic diagram of the doubler-last LO multiplier chain, which is similar to the 300-GHz CMOS TX [5]. An external LO signal, $LO^{1/6}$, at approximately 50 GHz, is first tripled, then split into differential signals by a rat-race balun, and then amplified by 150-GHz DAs. The differential cascaded DA was designed with a capacitive cross-coupling technique. The resulting signal undergoes a four-way balanced power splitting by a pair of

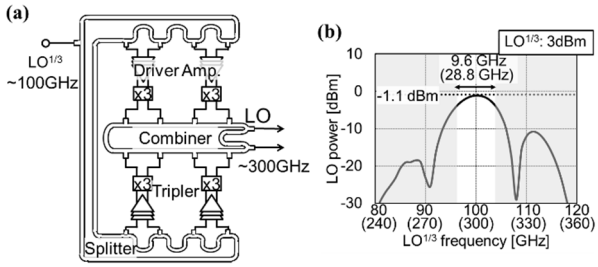


Fig. 8 (a) Schematic diagram of the tripler-last LO multiplier chain and (b) simulated result of frequency response of output power.

double-rat-race power splitters, and amplified by a five-stage DA and single-power-stage amplifiers that composed of the 32- and 64-um-wide transistors, respectively. The simulated gain, OP1dB, and P_{sat}, of the DA at 150 GHz are 24 dB, 6.1 dBm, and 9.4 dBm, respectively. The signal frequency is then doubled by the four single-ended doublers and the LO signal at approximately 300 GHz is obtained. Subsequent power combining is performed using a TL H tree, which is composed of two T-line sections. The signal inputs a rat-race balun for the differential signal to the balanced mixer. Figure 7 (b) shows the simulated frequency response of the 300-GHz output LO power. The output power is estimated to be −2.0 dBm with the input-referred 3-dB bandwidth (at $LO^{1/6}$) of 6.8 GHz, which corresponds to the output bandwidth at an RF of 40.8 GHz, from 274.8 GHz to 315.6 GHz. Further, the power consumption of 1.10 W is estimated.

Figure 8 (a) shows the schematic diagram of the tripler-last LO multiplier chain [18]. The LO multiplier consists of a rat-race-based four-way balanced power splitter, 100-GHz DAs, differential triplers upconverting the frequency of 100 GHz into 300 GHz, and a rat-race-based power combiner. The differential cascaded DA with a capacitive cross-coupling technique consists of a three-stage amplifier with 32-μm-wide transistors. Figure 8 (b) shows the simulated frequency response of the 300-GHz output LO power. The output power is estimated to be −1.0 dBm with the input-referred 3-dB bandwidth of 9.6 GHz, which corresponds to the output 3-dB bandwidth at an RF of 28.8 GHz, from 288.1 GHz to 311.7 GHz. However, the measured output power of 2.37 dBm was achieved by reducing the power and phase mismatch with a bias optimization system [18]. The power consumption was 0.41 W.

The output power of the doubler-last multiplier chain is slightly lower than that of the tripler-last multiplier chain because of the difference in the performance of the power combiner and DA. In addition, the power consumption of the tripler-last multiplier chain is superior owing to the small number of stages of the amplifier.

3. Results and Discussion

3.1 Performances of 300-GHz CMOS RXs

The performance evaluation of the 300-GHz RXs is performed by measuring the down-converted signals using a

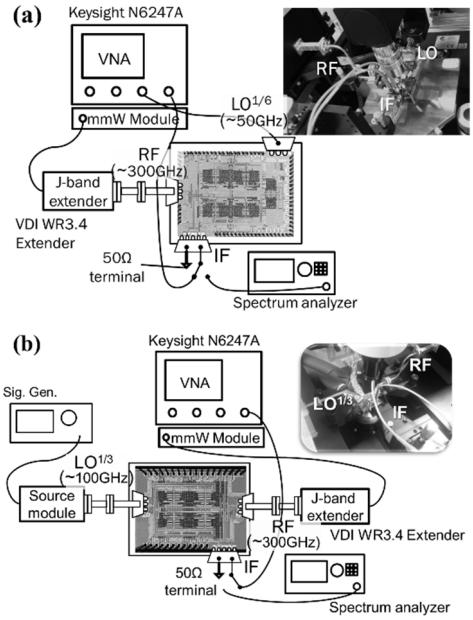


Fig. 9 Measurement setups of 300-GHz CMOS RXs with (a) doubler- and (b) tripler-last LO multipliers.

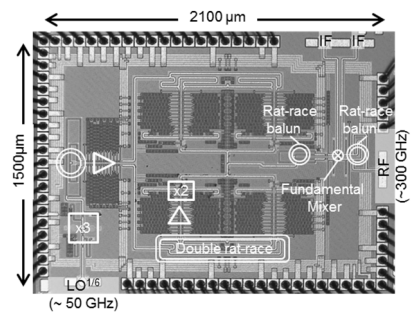


Fig. 10 Die micrograph of the 300-GHz CMOS receiver.

spectrum analyzer or vector network analyzer (VNA). An RF signal is generated to upconvert the signal from a VNA by a WR3.4-band frequency extender. The $LO^{1/n}$ signals supplied to the RXs with the doubler- and tripler-last LO multiplier chains are generated by a VNA and a signal generator with a WR10-band source module, respectively (shown in Figs. 9 (a) and (b)). High frequency signals are supplied via RF probes. One of the differential IF outputs is terminated with a 50-Ω load because an external balun was not available. The chips are mounted on a printed circuit board (PCB) for measurement. DC power is supplied through bond wires.

3.1.1 300-GHz RX with the Doubler-Last LO Multiplier Chain

The RX with a doubler-last LO multiplier chain was designed for the TSMC 40-nm 1P10M CMOS GP process. The chip area is 2.1 mm × 1.5 mm (shown in Fig. 10). The power consumption is 0.65 W, which is lower than that of the design. The complex DC supply line should be laid out

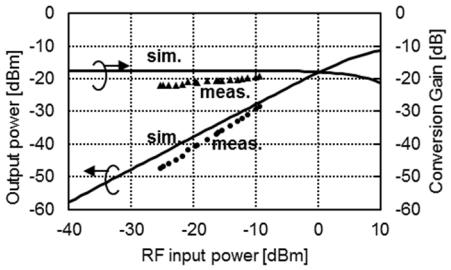


Fig. 11 Output power and conversion gain with an IF output of LSB 8-GHz signal vs RF input power. $LO^{1/6}$ power of 2 dBm is supplied.

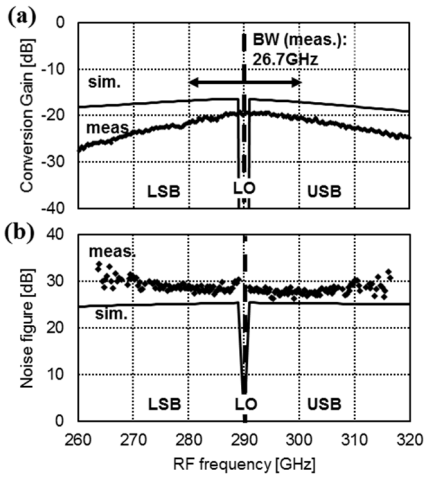


Fig. 12 (a) Conversion gain and (b) noise figure vs. RF frequency. The $LO^{1/6}$ signal with a frequency of 48.3 GHz and a power of 2 dBm are applied.

because of the large number of amplifier stages. The suppression of the power consumption is attributed to the voltage drop by the internal resistance of the DC supply lines.

Figure 11 shows the measured and simulated output power and conversion gain as functions of RF input power. The RF frequency is 294 GHz with an $LO^{1/6}$ of 50.3 GHz. It corresponds to an IF output of the lower sideband (LSB) at 8 GHz. The measured output power is lower than the simulated power by approximately 2 dB, which is attributed to the decrease in the LO power by the suppression of the DC supply. Figure 12 shows the RF frequency dependence on the conversion gain and noise figure. The peak of the measured conversion gain and the minimum of the noise figure are −19.5 dBm and 27 dB, respectively. The 3-dB bandwidth of the measured conversion gain is 26.7 GHz and is narrower than the simulated result by about 25 GHz. This appears to have been caused by the mismatches between the LO multiplier chain and RF mixer.

3.1.2 300-GHz RX with the Tripler-Last LO Multiplier Chain

The RX with a tripler-last LO multiplier chain was also designed for the TSMC 40-nm 1P10M CMOS GP process. The chip area is 1.76 mm × 1.29 mm (shown in Fig. 13).

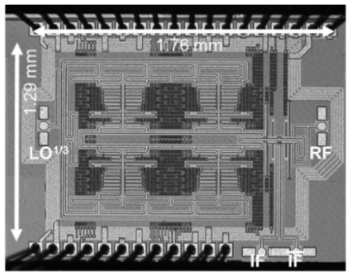


Fig. 13 Die micrograph of the 300-GHz CMOS receiver.

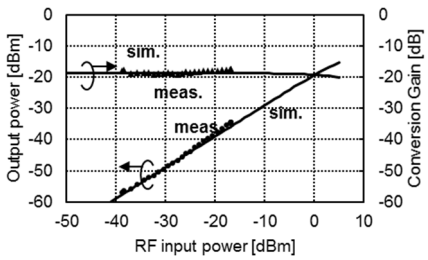


Fig. 14 Output power and conversion gain with an IF output of LSB 13-GHz signal vs. RF input power. $LO^{1/3}$ power of 0 dBm is supplied. Solid lines and dots show simulated and measured results, respectively.

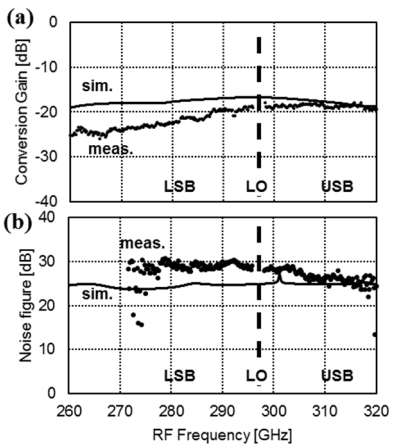


Fig. 15 (a) Output power, conversion gain, and noise figure vs. RF frequency. The $LO^{1/3}$ signal power is 0 dBm at a frequency of 96.5 GHz. Solid lines and dots show simulated and measured results, respectively.

The power consumption is 416 mW, which is almost similar to that of the design.

Figure 14 shows the measured and simulated output power and conversion gain as functions of RF input power. The RF frequency is 304 GHz and the $LO^{1/3}$ is 97 GHz. It gives an IF output of the upper sideband (USB) at 13 GHz. The simulated and measured output powers are in agreement and show good linearity. The conversion gain and noise figure according to the RF are shown in Fig. 15. Although the frequency deviation is slight, which is caused by the mismatch in the impedance matching, an output power of −18 dBm and a conversion gain of 25.5 dB are achieved. The 3-dB bandwidth is approximately 33 GHz at a cen-

ter frequency of 308 GHz. The high performance is attributed to the high performance of the tripler-last multiplier chain [14].

3.2 Wireless Performance of 300-GHz CMOS RXs

Figure 16 shows the measurement setup for short-range wireless communications. A TX test chip capable of up-converting a QAM signal to the RF range around 300 GHz is used, which can cancel the LO leak and suppress the images [6]. A pair of horn antennas separated by several centimeters is used for the free-space propagation of the RF signal. The received RF signal at a center frequency is fed to the RX chip via an RF probe. The $LO^{1/n}$ signal is supplied to the RX chip with a power of 2 dBm. The down-converted signal at a center frequency of 8 GHz is measured using a vector signal analyzer.

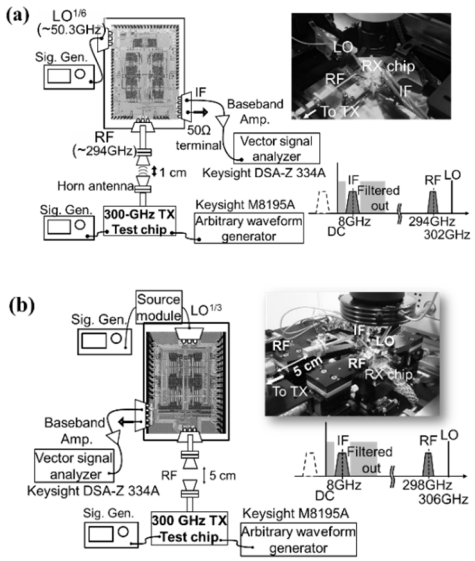


Fig. 16 Wireless measurement setups of 300-GHz CMOS RXs with (a) doubler- and (b) tripler-last LO multiplier chains.

Tables 2 and 3 show the measured signal constellations, error-vector magnitudes (EVM), bit error rate (BER), symbol rates, and data rates of 300-GHz CMOS RXs with the doubler- and tripler-last LO multiplier chains, respectively. The BER is estimated from the signal-to-noise ratio (SNR) calculated from the EVM [5] because the direct comparison of modulation quality and error performance is difficult between different modulations with the different number of symbols [19]. The wireless performances of both RXs are almost equivalent, and the highest data rate of 32 Gb/s is achieved with 16QAM. Further, the BERs of the RXs with doubler- and tripler-last LO multiplier chains are 9.3×10^{-5} and 3.2×10^{-4}, respectively. The good linearity as well as other performances, such as noise figure and conversion gain, of the RX would contribute to the achievement of QAMs.

Table 4 compares the state-of-the-art THz RXs. It is difficult to compare the performance directly because of the different RF frequencies, integration, and technology. How-

Table 2 Signal constellations, error-vector magnitudes, symbol rates, and data rates of 300-GHz CMOS RXs with doubler-last multiplier chain

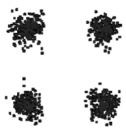
	QPSK	16QAM	32QAM
Constellation			
EVM	19.0%rms	12.2%rms	8.8%rms
BER	7.1×10^{-8}	9.3×10^{-5}	1.3×10^{-4}
Sym. rate	14 Gbaud	8 Gbaud	4 Gbaud
Data rate	28 Gb/s	32 Gb/s	20 Gb/s

Table 3 Signal constellations, error-vector magnitudes, symbol rates, and data rates of 300-GHz CMOS RXs with tripler-last multiplier chain

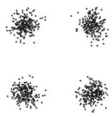
	QPSK	16QAM	32QAM
Constellation			
EVM	18.6%rms	13.4%rms	8.54%rms
BER	3.8×10^{-8}	3.2×10^{-4}	8.3×10^{-5}
Sym. date	10 Gbaud	8 Gbaud	4 Gbaud
Data rate	20 Gb/s	32 Gb/s	20 Gb/s

Table 4 Performance summary and comparison

Ref	[7]	[8]	[9]	[10]	[11]	[12]	This work	This work
Process	35-nm GaAs mHEMT	250-nm InP HBT	130-nm SiGe BiCMOS	130-nm SiGe HBT	90-nm CMOS	65-nm CMOS	40-nm CMOS	40-nm CMOS
RF (GHz)	228– 252	275–305†	227–245	315–328	200	240††	280–307	287–320
Conv. gain (dB)	3	-	11	-14	6.6	25	-19.5	-18
NF (dB)	10	-	16	36	29.9	15†††	27	25.5
Modulation	8PSK	ASK	QPSK / 16QAM / 64QAM	-	BPSK / QPSK	BPSK /QPSK	QPSK /16QAM /32QAM	QPSK /16QAM /32QAM
Data rate (Gb/s)	96	24	2.7 / 0.7 /1.0	-	4 / 2	10 / 16	28 / 32 / 20	20 / 32 / 20
DC (W)	-	0.284	0.87	0.216	0.063	0.26	0.65	0.42
Chip size (mm^2)	-	2.5	1.57	0.92	0.375	2	3.15	2.29
Integration	-	Antenna, LNA, Detector, BB amp.	Antenna, LNA, IQ Mixer, LO chain	SHM, LO chain	Mixer, IF amp.	Antenna, Mixer, IF amp., LO chain	Mixer, LO chain (DBL-last)	Mixer, LO chain (TRI-last)

† Estimated graphically, †† no description, ††† Simulated result,

ever, our RXs might be the first CMOS RX to encompass the frequency range above 275 GHz. The RX with the tripler-last multiplier chain has the advantage of lower power consumption with similar performance, compared with the RX with the doubler-last multiplier chain. However, with the design of a more power-efficient DA, a RX with higher performance would be realized using the doubler-last multiplier chain.

4. Conclusion

LNA-less 300-GHz RXs composed of a down-conversion mixer with the doubler-last and tripler-last LO multiplier chains are demonstrated using the 40-nm CMOS technology. The conversion gain of the RX with the doubler-last multiplier chain is −19.5 dB and its noise figure, 3-dB bandwidth, and power consumption are 27 dB, 27 GHz, and 0.65 W, respectively. The conversion gain of the RX with the tripler-last multiplier chain is −18 dB and its noise figure, 3-dB bandwidth, power consumption are 25.5 dB, 33 GHz, and 0.41 W, respectively. While the RX with the tripler-last multiplier chain has the advantage of low power consumption, the RX with the doubler-last multiplier chain could achieve a better performance by improving the DAs. The short-range wireless communication of both RXs is successfully demonstrated at a high data rate of 32 Gb/s with 16QAM. The development of THz CMOS technology is still at the rudimentary stage; nevertheless, these results are encouraging.

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References

[1] T. Kürner, IEEE 802.15-10-0320-02-0000-Tutorial_Igthz.
[2] M. Fujishima, "Channel allocation of 300GHz band for fiber-optic-speed wireless communication," URSI Asia-Pacific Radio Sci. Conf., Seoul, South Korea, pp.330–333, Aug. 2016.
[3] M. Fujishima and S. Amakawa, "Integrated-circuit approaches to THz communications: Challenges, advances, and future prospects," IEICE Trans. Fundamentals, vol.E100-A, no.2, pp.516–523, Feb. 2017.
[4] K. Katayama, K. Takano, S. Amakawa, S. Hara, A. Kasamatsu, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 300 GHz CMOS transmitter with 32-QAM 17.5 Gb/s/ch capability over six channels," IEEE J. Solid-State Circuits, vol.51, no.12, pp.3037–3048, Dec. 2016.
[5] K. Takano, K. Katayama, S. Amakawa, T. Yoshida, and M. Fujishima, "Wireless digital data transmission from a 300 GHz CMOS transmitter," Electron. Lett., vol.52, no.15, pp.1353–1355, July 2016.
[6] K. Takano, S. Amakawa, K. Katayama, S. Hara, R. Dong, A. Kasamatsu, I. Hosako, K. Mizuno, K. Takahashi, T. Yoshida, and M. Fujishima, "A 105Gb/s 300GHz CMOS transmitter," Int. Solid-State Circuits Conf., San Francisco, CA, USA, pp.308–309, Feb. 2017.
[7] I. Kallfass, F. Boes, T. Messinger, J. Antes, A. Inam, U. Lewark, A. Tessmann, and R. Henneberger, "64 Gbit/s transmission over 850 m fixed wireless link at 240 GHz carrier frequency," J. Infrared Milli. Terahz. Waves, vol.36, no.2, pp.221–223, Feb. 2015.
[8] H.-J. Song, J.-Y. Kim, K. Ajito, M. Yaita, and N. Kukutsu, "Fully integrated ASK receiver MMIC for terahertz communications at 300 GHz," IEEE Trans. Terahertz. Sci. Tech., vol.3, no.4, pp.445–452, July 2013.
[9] N. Sarmah, J. Grzyb, K. Statnikov, S. Malz, P.R. Vazquez, W. Foerster, B. Heinemann, and U.R. Pfeiffer, "A fully integrated 240-GHz direct-conversion quadrature transmitter and receiver chipset in SiGe technology," IEEE Trans. Microw. Theory Tech., vol.64, no.2, pp.562–574, Feb. 2016.
[10] E. Öjefors, B. Heinemann, and U.R. Pfeiffer, "Subharmonic 220- and 320-GHz SiGe HBT receiver front-ends," IEEE Trans. Microw. Theory Tech., vol.60, no.5, pp.1397–1404, May 2012.
[11] M. Tytgat, M. Steyaert, and P. Reynaert, "A 200 GHz downconverter in 90 nm CMOS," in Proc. Euro. Solid State Device Res. Conf. (ESSCIRC) 2011, Helsinki, Finland, pp.239–242, Sept. 2011.
[12] S.V. Thyagarajan, S. Kang, and A.M. Niknejad, "A 240 GHz fully integrated wideband QPSK receiver in 65 nm CMOS," IEEE J. Solid-State Circuits, vol.50, no.10, pp.2268–2280, Oct. 2015.
[13] S. Hara, K. Katayama, K. Takano, R. Dong, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "A 32Gbit/s 16QAM CMOS Receiver in 300GHz Band," 2017 IEEE International Microwave Symposium (IMS2017), pp.1–4, June 2017.
[14] S. Hara, K. Katayama, K. Takano, R. Dong, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "A 416-mW 32-Gbit/s 300-GHz CMOS Receiver," 2017 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), pp.65–67, Aug. 2017.
[15] S. Mass, "Microwave Mixers," Boston: Artech House, 1993.
[16] M. Bashir and A. Bhardwaj, "Comparative Study of Broadband RF Subharmonic Mixers in Submicron Technology," International Conference on Recent Advances in Communication, VLSI & Embedded Systems 2014 (ICRACVES 2014), pp.47–51, Dec. 2014.
[17] S. Hara, K. Katayama, K. Takano, I. Watanabe, N. Sekine, A. Kasamatsu, T. Yoshida, S. Amakawa, and M. Fujishima, "Compact 141-GHz differential amplifier with 20-dB peak gain and 22-GHz 3-dB bandwidth," IEICE Trans. Electron., vol.E99-C, no.10, pp.1156–1163, Oct. 2016.
[18] K. Katayama, K. Takano, S. Amakawa, T. Yoshida, and M. Fujishima, "2.37-dBm-output 288–310 GHz frequency multiplier in 40 nm CMOS," in Proc. IEEE Radio-Frequency Integration Technology (RFIT) 2017, Seoul, South Korea, pp.28–30, Aug. 2017.
[19] M. Vigilante, E. McCune, and P. Reynaert, "To EVM or two EVMs?," IEEE SSC Magazine, vol.9, no.3, pp.36–39, Summer 2017.

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