Detector Control System of the new Muon Forward Tracker at ALICE

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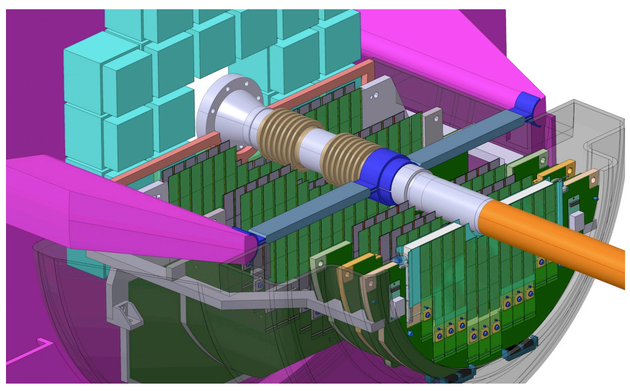
ALICE Forward Upgrade in LHC Run 3

ALICE plans major detector upgrades in LHC Run 3 from 2021. The forward muon arm will be newly equipped with a precise silicon pixel detector in front of the hadron absorber, along with a much enhanced data rate capability, to enable separation of prompt and non-prompt components of single- and di-muons and an improvement of di-muon invariamant mass resolution, as well as minimum-bias readout of Pb-Pb collisions at up to 50 kHz. New and high precision measurements will be enabled for open charm and beauty hadrons, J/Ψ, Ψ(2S), and Υ's, and low-mass di-muons, opening unique physics programs at LHC.

Muon Forward Tracker

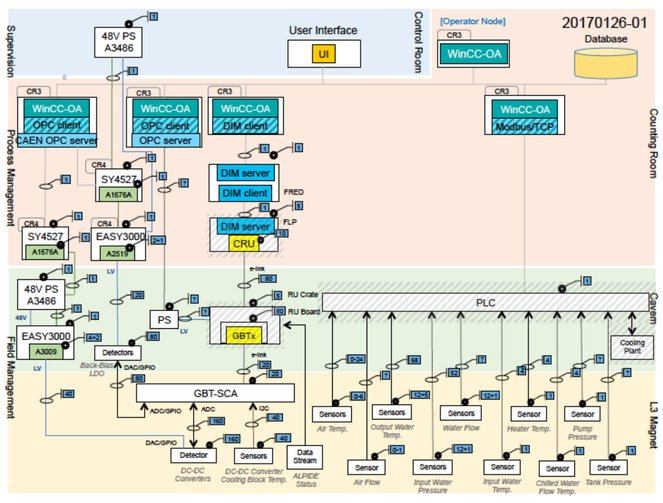


MFT (muon forward tracker) has 5 double-sided layers of silicon pixel detectors based on the MAPS technology. Each "half plane" is divided into 4 zones, which is the minimum granule for detector control such as power distribution and interlock.

← A sketch of the lower half of MFT. It consists of 5 layers of detectors (half disks), each with 2 sensor planes (half planes) sandwiching a support structure with water cooling pipes. Half planes on the last 2 layers also carry power distribution components, such as DC-DC converters, while those for the first 3 layers are integrated on a separate power unit board.

Hardware Architectures

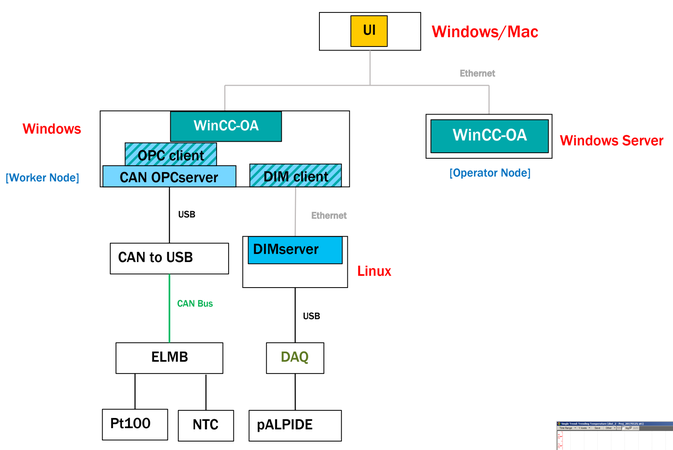
The hardware architecture design is summarized in the diagram on the right, called a user requirements document. The main part of the system includes control and monitoring of 3 series (for analog/digital/bias) of low voltage power for the pixel sensors, power for the readout electronics boards, and the water cooling unit, and monitoring of various sensors and status of the pixel sensor chips (via CRU). Configuration of the chips is handled in the data stream apart from the DCS.

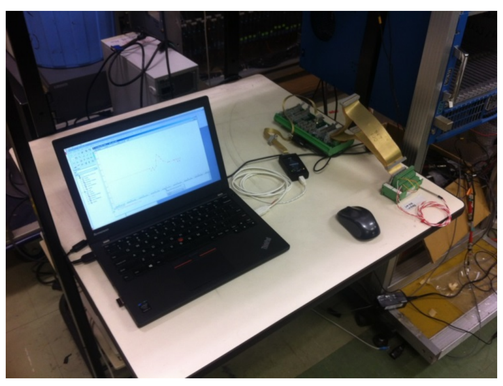


→ The hardware architecture of MFT. The background colors show physical locations, *e.g.* inside of the ALICE detector magnet, the experimental floor, the underground counting rooms, and the control room on the surface. Each box denotes a device, with its number in small blue box. The lines are either wires, optical data links, or ethernet.

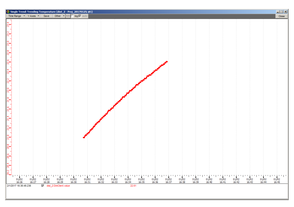
Test System at Hiroshima

A test system of the MFT DCS has been established at Hiroshima University, Japan, with a help from the ALICE central DCS team at CERN. It is meant to be a small scale but nearly complete prototype, with multi nodes on WinCC-OA distributed project. The worker node communicates with devices via OPC (OLE for process control) and DIM (distributed information management system). An example below shows how temperature sensors on the final prototype of the pixel sensor (pALPIDEv3) are read out and monitored, mimicking the data stripping at CRU for DCS. One of the missing pieces is GBT-SCA, whose production version is not yet available as of January, 2017.





↑ Schematics and a photo of the DCS test system at Hiroshima, based on WinCC-OA distributed project.



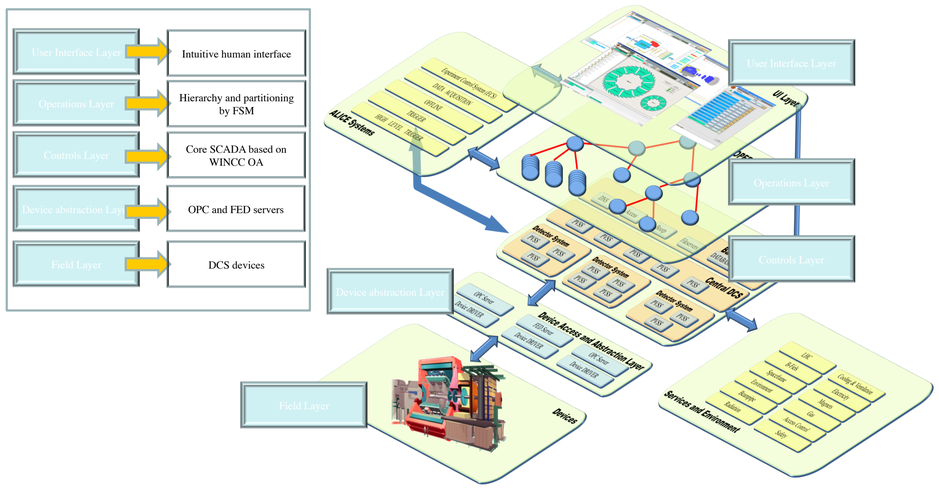
→ A working example of the test system. Temperature of the pixel sensor prototype (pALPIDE) is read out and monitored from the operator node.

Plan and Schedule

MFT is scheduled to be installed into ALICE in LHC Long Shutdown 2 in 2019-2020. The detector construction and assembly hence shoot for finishing by the end of 2018. The DCS development is mostly planned in 2017, with an interface to the water cooling system, to be finalized in 2018, followed by installation into ALICE in 2019 and commissioning in 2020.

Detector Control System in ALICE Run 3

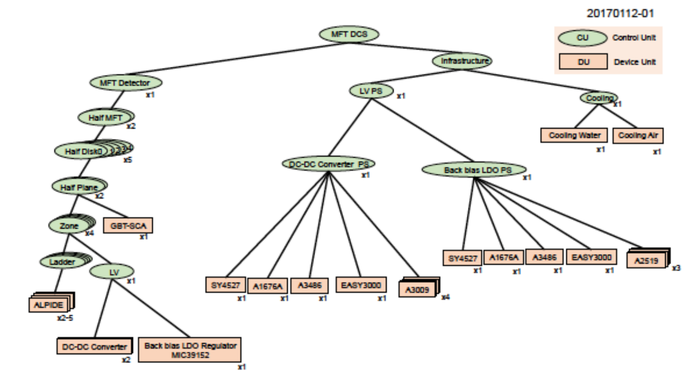
ALICE updates many of the architectures for its DCS (detector control system) in Run 3. It is a multi-layered system with the core of SCADA (supervisory control and data acquisition) based on Siemens WinCC-OA, topped with CERN JCOP (joint controls project) framework. On the lowest field layer, GBT-SCA (giga bit transfer slow control adapter) will replace ELMB (embedded local monitor board) being used for the existing detector subsystems. An additional data path exists, *e.g.* for status of pixel sensor chips, to be read out in the event data stream and stripped for the DCS at CRU (common readout unit).



↑ Schematics of ALICE detector control system in Run 3. It starts with the lowest field layer with hardware drivers, then the device abstraction layer with OPC, DIM, etc., the controls layer with SCADA on WinCC-OA, operations layer with FSM on JCOP, and finally the user interface layer.

Finite State Machines

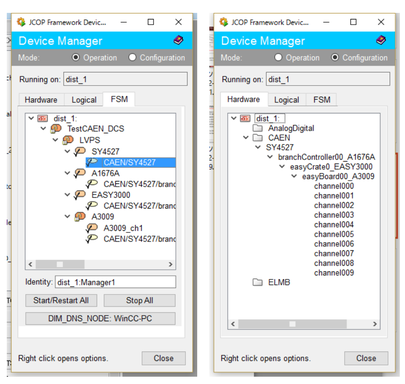
ALICE DCS is based on FSM (finite state machine) in JCOP framework. The tree structure has been identified for entire MFT, along with the state diagram of each node and their dependency.



↑ The logical tree structure of MFT. The FSM nodes are categorized into control units (green ellipses) and device units (pink rectangles).

Implementation of Control Logics

Implementation of FSM into JCOP framework is in progress, based on the MFT logic design. Communication between nodes has been established. FSM will be also implemented onto the DCS test system.



← FSM trees implemented in JCOP framework, in terms of logical structure (left) and hardware structure (right).

→ Synchronization table of the top node of MFT DCS in JCOP framework.

SynchronizationTable_MFT_DCS		
MFT_DCS	MFT_Detector	Infrastructure
OFF	OFF	NOT_READY
STANDBY	STANDBY	NOT_READY
DOWNLOADING	DOWNLOADING	DOWNLOADING
STBY_CONFIGURED	STBY_CONFIGURED	STBY_CONFIGURED
CALIBRATING	CALIBRATING	STBY_CONFIGURED
BEAMTUNING	STBY_CONFIGURED	STBY_CONFIGURED
MOVING_READY	MOVING_READY	MOVING_READY
MOVING_STBY_CONF	MOVING_STBY_CONF	MOVING_STBY_CONF
READY	READY	READY
READY_LOCKED	RUNNING	READY
		WARNING
ERROR		ERROR
NO_CONTROL		NO_CONTROL
PWS_FAILURE		PWS_FAILURE
INTERLOCK		INTERLOCK
INTERLOCK_WENT		INTERLOCK_WENT
MIXED	MIXED	
	WARNING	
ERROR	ERROR	
NO_CONTROL	NO_CONTROL	
INTERLOCK	INTERLOCK	
INTERLOCK_WENT	INTERLOCK_WENT	

Summary and Prospects

ALICE Muon Forward Tracker (MFT) is a new silicon pixel detector and a part of the upgrades toward LHC Run 3 starting in 2021. Its DCS is under design and implementation based on the new architecture choices at ALICE. A test system has been established at Hiroshima University, meant to become a small scale but complete prototype. Development is in progress both on the hardware and logic fronts. A key component, GBT-SCA, is expected to arrive in the near future, to allow a complete configuration and monitoring chain. A hardware interlock is also under design, to be implemented in the existing LHC device protection system.

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